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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,278	06/29/2001	Mark Anders	10559-403001 / P10340	7194

20985 7590 09/21/2004

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EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,278	ANDERS ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al., hereinafter Wada (U.S. 6,225,846) in view of Fujita et al., hereinafter Fujita (U.S. 6,215,159), all previously cited.

Regarding claim 1, Wada discloses in figure 1 an input gate including an input transistor P3 having an input node L6 and an output node shown as "out", further disclosing a plurality of transistors coupled between the input node and the output node.

Wada dose not disclose two or more clocked input gates.

Fujita teaches that pluralities of clock signals are applied to the transistors shown in figure 5A. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signals to the gate of the transistor in Wada's invention, since it is known in the art that clock signals are used to operate MOS transistors in order to control the desired voltage at their output according to a time interval.

Regarding claim 2, Wada discloses in figure 1 the transistors include a PMOS transistor P3 coupled to E3 and an NMOS transistor N4 coupled to Vss, the input transistor N3 being connected between said PMOS and NMOS transistors.

3. Claims 3-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Fujita as applied to claim 1 above, and further in view of Rossi et al., hereinafter Rossi, previously cited (U.S. 6,069,513).

Regarding claims 3 and 4, Wada discloses in figure 1 an intermediate node coupled to one of a source and a drain of the input transistor N3; and an output inverter 2 having an output coupled to the output node and an input coupled to the intermediate node.

Wada in view of Fujita dose not disclose a first transistor having a gate coupled to the input node and one of a source and a drain connected to the intermediate node; and a second transistor connected in series with the first transistor, said second transistor having one of a source and a drain connected to a voltage supply.

Rossi discloses in figure 6 a first transistor M4 having a gate coupled to the input node T and one of a source and a drain connected to an intermediate node B; and a second transistor M3 connected in series with the first transistor, the second transistor having one of a source and a drain connected to a voltage supply vdd. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include these transistors in the invention of Wada in view of Fujita in order to have a pull up transistor at the intermediate node.

Regarding claims 5-10, Wada discloses a feedback inverter 2 where the input of the inverter connected to the intermediate node and an output coupled to a gate of the second transistor P3.

4. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada and Fujita in view of Rossi and further in view of Gillingham et al., hereinafter Gillingham (U.S. Patent 6,510,503), previously cited.

Wada and Fujita in view of Rossi disclose the limitations in the claims, as discussed above, except for a dynamic bus.

Gillingham teaches at column 7, lines 12-22, that using a repeater on a main bus creates a sub-bus on the main bus, and therefore, increases the latency of the device as a whole. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the repeater in the dynamic bus of Wada in view of Fujita and Rossi, as Gillingham teaches, in order to make the connection between the drivers and the flip flops, while creating a sub-bus on the dynamic bus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

LONG PHAM
PRIMARY EXAMINER